AMENDMENTS TO THE CLAIMS

This listing of claim will replace all prior versions and listings of claim in the application.

1. (original) A method for reading non-volatile memory arranged in columns and rows, comprising the steps of:

selecting a word-line WLn to be read;

reading an adjacent word line (WLn+1) written after word line WLn; and

reading the selected bit in word line WLn by selectively adjusting at least one read parameter.

2. (original) The method of claim 1 wherein the read parameter is the sense voltage.

3. (original) The method of claim 2 wherein the step of reading the bit includes increasing the sense voltage.

4. (original) The method of claim 3 wherein the step of increasing the sense voltage includes increasing the sense voltage by an amount equal to a fraction of the maximum coupling effect of the adjacent bit on the selected bit.

5. (original) The method of claim 4 wherein the fraction is one-half.

6. (original) The method of claim 1 wherein the read parameter is the pre-charge voltage.

7. (original) The method of claim 1 wherein the step of reading the bit includes decreasing the pre-charge voltage.

8. (original) The method of claim 7 wherein the step of decreasing the pre-charge voltage includes decreasing the sense voltage by an amount equal to a fraction of the maximum coupling effect of the adjacent bit on the selected bit.

9. (original) The method of claim 1 wherein the method includes the step, following the step of reading an adjacent word line, of determining whether a bit in word line WLn+1 adjacent to the selected bit has a threshold voltage above a check voltage.

10. (original) The method of claim 9 wherein said step of reading the selected bit occurs only if said bit in word line WLn+1 is greater than the check voltage.

11. (original) The method of claim 10 wherein the check voltage is one half of the voltage threshold distribution.

12. (original) The method of claim 1 wherein the bits hold a multi-state memory, the step of reading an adjacent word line includes determining the threshold voltage state of the bit.

13. (original) The method of claim 12 wherein the step of reading includes reading the bit at least three times.

14. (original) The method of claim 13 wherein the step of reading the selected bit includes decreasing the sense voltage by an amount equal to the coupling effect of the adjacent bit on the selected bit.

15. (original) The method of claim 13 wherein the step of reading the selected bit includes increasing the pre-charge voltage by an amount equal to the coupling effect of the adjacent bit on the selected bit.

16. (original) The method of claim 1 wherein said at least one read parameter includes both the pre-charge voltage and the sense voltage.

17. (original) A method for reading non-volatile memory arranged in columns and rows, comprising the steps of:

determining a selected bit to be read in a first word-line;

reading an adjacent word line written after the first word line;

determining whether a bit adjacent to the selected bit has a threshold voltage greater than a check value; and

if the selected bit has a threshold voltage greater than the check value, reading the selected bit in word line by selectively adjusting at least one read parameter.

18. (original) The method of claim 17 wherein the read parameter is the sense voltage.

19. (original) The method of claim 18 wherein the step of reading the bit includes increasing the sense voltage.

20. (original) The method of claim 19 wherein the step of increasing the sense voltage includes increasing the sense voltage by an amount equal to one-half of the maximum coupling effect of the adjacent bit on the selected bit.

21. (original) The method of claim 17 wherein the read parameter is th pre-charge voltage.

22. (original) The method of claim 17 wherein the step of reading the bit includes decreasing the pre-charge voltage.

23. (original) The method of claim 22 wherein the step of decreasing the pre-charge voltage includes decreasing the sense voltage by an amount equal to one-half of the maximum coupling effect of the adjacent bit on the selected bit.

24. (original) The method of claim 17 wherein the check voltage is one half of the voltage threshold distribution of a multi-state cell array.

25. – 32. (withdrawn).